What is claimed is:

1. A method for forming a bump comprising the steps of:

forming a resist layer so that a through-hole formed therein is located on a pad; and

forming a metal layer to be electrically connected to the pad conforming to the shape of the through-hole,

wherein the metal layer is formed so as to have a shape in which is formed a region for receiving a soldering or brazing material.

2. The method for forming a bump according to claim 1,

wherein the resist layer is formed so as to have a projection on the inner side of the through-hole.

3. The method for forming a bump according to claim 1,

wherein the resist layer is formed so that part of the resist layer remains at the center of the through-hole.

4. The method for forming a bump according to claim 1,

wherein a plurality of the through-holes are formed in the resist layer so that at least a part of each of the through-holes is superposed on the pad, and

a plurality of the metal layers are formed, each of the plurality of the metal layers conforming to each of the through-holes to form the region for receiving the soldering or brazing material between the adjacent metal layers of the

plurality of the metal layers on the pad.

5. The method for forming a bump according to claim 1,

wherein the metal layer comprises first and second metal layers,

wherein the first metal layer is formed in a state in which the resist layer is formed, and the second metal layer is formed on the first metal layer.

6. The method for forming a bump according to claim 1,

wherein the metal layer comprises first and second metal layers,

wherein the first metal layer is formed in a state in which the resist layer is formed, and

after removing the resist layer, the second metal layer is formed so as to cover a surface of the first metal layer.

7. The method for forming a bump according to claim 5,

wherein the pad is covered with an insulating film,

the resist layer is formed on the insulating film,

an opening for exposing at least part of the pad is formed in the insulating film after forming the through-hole in the resist layer, and

the first metal layer is formed on the pad in a state in which the resist layer is formed.

8. The method for forming a bump according to claim 6,

wherein the pad is covered with an insulating film,

the resist layer is formed on the insulating film,

an opening for exposing at least part of the pad is formed in the insulating film after forming the through-hole in the resist layer, and

the first metal layer is formed on the pad in a state in which the resist layer is formed.

9. The method for forming a bump according to claim 5, wherein the first and second metal layers are formed by electroless plating.

10. The method for forming a bump according to claim 6, wherein the first and second metal layers are formed by electroless plating.

11. The method for forming a bump according to claim 5, wherein the first metal layer is formed of a material containing nickel.

12. The method for forming a bump according to claim 6, wherein the first metal layer is formed of a material containing nickel.

13. The method for forming a bump according to claim 5, wherein the second metal layer is formed of a material containing gold.

14. The method for forming a bump according to claim 6,

wherein the second metal layer is formed of a material containing gold.

15. A method of fabricating a semiconductor device comprising the steps of:

bonding a plurality of metal layers to a plurality of leads through a soldering or brazing material, each of the metal layers formed on each of a plurality of pads of a semiconductor chip , each of the metal layers having a shape in which is formed a region for receiving the soldering or brazing material,

wherein the soldering or brazing material, when melted, is allowed to flow into the region of each of the metal layers for receiving the soldering or brazing material so as not to spread onto an adjacent pad of the plurality of pads.

16. The method of fabricating a semiconductor device according to claim 15,

wherein at least one depression is formed in a side of one of the metal layers, and

the soldering or brazing material is allowed to flow into the depression.

17. The method of fabricating a semiconductor device according to claim 15,

wherein one of the metal layers is formed so that a

depression which is provided in the direction of the height of the metal layers is formed at the center, and

the soldering or brazing material is allowed to flow into the depression.

18. The method of fabricating a semiconductor device according to claim 15,

wherein two or more metal layers of the plurality of metal layers are formed so as to be connected to one of the pads, and

the soldering or brazing material is allowed to flow into a region formed between the adjacent metal layers of the plurality of metal layers on one of the pads.

19. A semiconductor device fabricated by the fabrication method according to claim 15.

20. A semiconductor chip comprising a plurality of pads, and a metal layer disposed on each of the pads which is formed to have a shape in which is formed a region for receiving a soldering or brazing material.

21. The semiconductor chip according to claim 20,

wherein at least one depression is formed in a side of the metal layer.

22. The semiconductor chip according to claim 20,

wherein a depression which is provided in the direction

of the height of the metal layer is formed at the center of the metal layer.

23. The semiconductor chip according to claim 20, wherein two or more the metal layers are formed on one of the pads.

24. A semiconductor device comprising:

a semiconductor chip having a plurality of pads;

a metal layer disposed on each of the pads, the metal layer formed to have a shape in which is formed a region for receiving a soldering or brazing material; and

a plurality of leads,

wherein the metal layer is bonded to one of the leads through the soldering or brazing material, and part of the soldering or brazing material is put in the region for receiving the soldering or brazing material.

25. The semiconductor device according to claim 24, wherein at least one depression is formed in a side of the metal layer, and

the soldering or brazing material is put in the depression.

26. The semiconductor device according to claim 24, wherein a depression which is provided in the direction of the height of the metal layer is formed at the center of the

metal layer, and

the soldering or brazing material is put in the depression.

27. The semiconductor device according to claim 24,

wherein two or more the metal layers are formed on one of the pads, and

the soldering or brazing material is put in a region formed between adjacent metal layers of the two or more the metal layers on one of the pads.

28. A circuit board on which is mounted the semiconductor device according to claim 24.

29. An electronic instrument comprising the semiconductor device according to claim 24.